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10/712,164	11/13/2003	Hyoung-Rac Kim	SAM-0504	8205

7590 02/08/2007
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EXAMINER

DHARIA, PRABODH M

ART UNIT	PAPER NUMBER
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2629

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Art Unit: 2629

1. **Status:** Please all replies and correspondence should be addressed to examiner's new art unit 2629. Receipt is acknowledged of papers submitted on 12-08-2006 under amendments, which have been placed of record in the file. Claims 1-13 are pending in this action.

Response to Amendment

2. The amendment filed 12-08-2006 do not introduce nay new matter into the disclosure. The added material, which is supported by the original disclosure. The abstract and drawings are corrected per objection and there fore objection to abstract and drawing is withdrawn.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claim12 is rejected under 35 U.S.C. 102(e) as being anticipated by Morita (US 2002/0196243 A1).

Art Unit: 2629

Regarding Claim 12, Morita teaches teaches a driving method of a super twisted nematic (STN) liquid crystal display (LCD) driver using an nFRC (page 3, paragraph 63, page 15, paragraphs 300-308, page 16, paragraphs 311-317) method, wherein a polarity of the STN LCD is inverted in each frame (page 3, paragraph 63, page 15, paragraphs 300-308, page 16, paragraphs 311-317).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 1-11 and 13 rejected under 35 U.S.C. 103(a) as being unpatentable over Morita (US 2002/0196243 A1) in view of Tajima et al. (US 6,249,265 B1).

Regarding Claims 1, Morita teaches a super twisted nematic (STN) (page 3, paragraph 63) liquid crystal display (LCD) driver (see figure 1, page 7, paragraphs 138,139, page 3, paragraph 63, page 15, paragraphs 300-308, page 16, paragraphs 311-317, paragraphs 326-333, page 15, paragraphs 291-297) comprising: a sub frame counter (page 15, paragraphs 291-297, page 16, paragraphs 311-317), which counts the number of sub frames in response to a clock signal (page 15, paragraphs 291-297, page 16, paragraphs 311-317, 327), and generates a sub frame flag (indication of counting done and reset signal generation by the counter) signal every time each sub frame is counted (page 16, paragraph 327); an N clock counter, which receives an N-line signal and

Art Unit: 2629

generates an N-line flag signal every time the number of N-line counted is N in response to the clock signal (page 16, paragraphs 326,327); a frame counter, which receives a frame rate control (FRC) selection signal (page 16, paragraph 326), counts the number of the sub frame flag signal, and generates a frame flag signal every time the number of the sub frame flag signal counted is n (page 16, paragraphs 326-333); and a liquid crystal polarity inversion signal generator, which receives one of the sub frame flag signal, the N-line flag signal, and the frame flag signal in response to the FRC selection signal, and generates a liquid crystal polarity inversion signal that inverts a polarity of an STN LCD (page 3, paragraph 63, page 15, paragraphs 300-308, page 16, paragraphs 311-317, paragraphs 326-333, page 15, paragraphs 291-297).

However, Morita fails to recite and specifically disclose LCD comprising a sub frame counter, which counts the number of sub frames in response to a clock signal and receives flag signal from the sub-frame counter, and a frame, which receives a frame rate control (FRC) selection signal to process display data.

However, Tahjima et al. teaches LCD (Col. 1, Line 40, Col. 37, Lines 61-63), comprising a sub frame counter (Col. 6, Lines 64, Col. 7, Line 10), which counts the number of sub frames in response to a clock signal (Col. 6, lines 61-65, Col. 7, lines 1-5), and receives flag signal from the sub-frame counter (Col. 6, lines 61-65, Col. 7, lines 1-5), and receives flag signal from the sub-frame counter (Col. 6, lines 61-65, Col. 7, lines 1-5), a frame which receives a frame rate control (FRC) selection signal to process display data for a moving image displayed on a display panel (Col. 26, Lines 23-50 teaches since sub-frames are used to process video the frame counter selects this gray-scale adjustment means including an intensity data arrangement switching means and a

Art Unit: 2629

frame counter, which select, from a number of sub-frame groups (SF1 to SFn) having mutually differing sustained discharge periods (intensity weights), a number of sub-frames having predetermined numbers to make up one frame).

Thus it would have been obvious to one in the ordinary skill in the art at the time of invention was made to incorporate the teaching of Tahjima et al. in the teaching of Morita to be able to drive liquid crystal display device capable of efficiently supplying information and providing a correct gradation display without flickering (Col. 43, Lines 18-33).

Regarding Claims 2, Morita teaches the STN LCD driver further comprises: a column driver, which receives data and generates a segment voltage that drives a column electrode of the STN LCD in response to a level of the liquid crystal polarity inversion signal; and a row driver, which receives a row selection signal and generates a row voltage that drives a row electrode of the STN LCD in response to the level of the liquid crystal polarity inversion signal (page 12, paragraphs 247,248, page 13, paragraphs 249-256).

Regarding Claim 3, Morita teaches the FRC selection signal has information on whether a driving method of the STN LCD is an nFRC method, where n is a natural number (page 3, paragraph 63, page 15, paragraph 306-308, page 16, paragraphs 326,327).

Art Unit: 2629

Regarding Claim 4, Morita teaches the N-line signal has information used to divide a frame into N sub frames, where N is a natural number (page 16, paragraph 326,327).

Regarding Claim 5, Morita teaches a super twisted nematic (STN) (page 3, paragraph 63) liquid crystal display (LCD) driver (see figure 1, page 7, paragraphs 138,139, page 3, paragraph 63, page 15, paragraphs 300-308, page 16, paragraphs 311-317, paragraphs 326-333, page 15, paragraphs 291-297) method comprising: (a) counting the number of sub frames in response to a clock signal and generating a sub frame flag signal every time each frame is counted (page 15, paragraphs 291-297, page 16, paragraphs 311-317, 327); (b) receiving an N-line signal and generating an N-line flag signal in response to input of the clock signal every time the number of N-line counted is N in response to the clock signal (page 16, paragraph (page 16, paragraphs 326,327); (c) receiving a frame rate control (FRC) selection signal, counting the number of sub frame flag signals, and generating a frame flag signal every time the number of sub frame flag signals counted is n (page 16, paragraphs 326-333); and (d) selecting one of the sub frame flag signal, the N-line flag signal, and the frame flag signal in response to the FRC selection signal, and generating a liquid crystal polarity inversion signal that inverts a polarity of the STN CLD (page 3, paragraph 63, page 15, paragraphs 300-308, page 16, paragraphs 311-317, paragraphs 326-333, page 15, paragraphs 291-297).

However, Morita fails to recite and specifically disclose LCD comprising a sub frame counter, which counts the number of sub frames in response to a clock signal and

Art Unit: 2629

receives flag signal from the sub-frame counter, and a frame, which receives a frame rate control (FRC) selection signal to process display data.

However, Tahjima et al. teaches LCD (Col. 1, Line 40, Col. 37, Lines 61-63), comprising a sub frame counter (Col. 6, Lines 64, Col. 7, Line 10), which counts the number of sub frames in response to a clock signal (Col. 6, lines 61-65, Col. 7, lines 1-5), and receives flag signal from the sub-frame counter (Col. 6, lines 61-65, Col. 7, lines 1-5), and receives flag signal from the sub-frame counter (Col. 6, lines 61-65, Col. 7, lines 1-5), a frame which receives a frame rate control (FRC) selection signal to process display data for a moving image displayed on a display panel (Col. 26, Lines 23-50 teaches since sub-frames are used to process video the frame counter selects this gray-scale adjustment means including an intensity data arrangement switching means and a frame counter, which select, from a number of sub-frame groups (SF1 to SFn) having mutually differing sustained discharge periods (intensity weights), a number of sub-frames having predetermined numbers to make up one frame).

Thus it would have been obvious to one in the ordinary skill in the art at the time of invention was made to incorporate the teaching of Tahjima et al. in the teaching of Morita to be able to drive liquid crystal display device capable of efficiently supplying information and providing a correct gradation display without flickering (Col. 43, Lines 18-33).

Regarding Claim 6, Morita teaches the driving method of the STN LCD driver (see figure 1, page 7, paragraphs 138,139, page 3, paragraph 63) further comprises: (e) receiving data and generating a segment voltage that drives a column electrode of the

Art Unit: 2629

STN LCD in response to the level of the liquid crystal polarity inversion signal; and (f) receiving a row selection signal and, in response to the level of the liquid crystal polarity inversion signal, generating a row voltage that drives a row electrode of STN LCD (page 12, paragraphs 247,248, page 13, paragraphs 249-256).

Regarding Claim 7, Morita teaches the FRC selection signal has information on whether a driving method of the STN LCD is an nFRC method, and the n is a natural number (page 3, paragraph 63, page 15, paragraph 306-308, page 16, paragraphs 326,327).

Regarding Claim 8, Morita teaches the N-line signal has information used to divide a frame into N sub frames, and the N is a natural number (page 16, paragraph 326,327).

Regarding Claim 9, Morita teaches a driving method of a super twisted nematic (STN) liquid crystal display (LCD) driver (page 3, paragraph 63), the driving method comprising: (a) determining whether a frame rate control (FRC) selection signal is in accordance with an nFRC method (page 15, paragraph 306-308, page 16, paragraphs 326,327); (b) counting the number of sub frames (page 15, paragraphs 300-308); and (c) generating a liquid crystal polarity inversion signal that inverts a polarity of the STN LCD if the number of sub frames is n (page 32, paragraph 63, page 15, paragraphs 300-308, page 16, paragraphs 311-317).

However, Morita fails to recite and specifically disclose LCD comprising a sub frame counter, which counts the number of sub frames in response to a clock signal and receives flag signal from the sub-frame counter, and a frame, which receives a frame rate control (FRC) selection signal to process display data.

However, Tahjima et al. teaches LCD (Col. 1, Line 40, Col. 37, Lines 61-63), comprising a sub frame counter (Col. 6, Lines 64, Col. 7, Line 10), which counts the number of sub frames in response to a clock signal (Col. 6, lines 61-65, Col. 7, lines 1-5), and receives flag signal from the sub-frame counter (Col. 6, lines 61-65, Col. 7, lines 1-5), and receives flag signal from the sub-frame counter (Col. 6, lines 61-65, Col. 7, lines 1-5), a frame which receives a frame rate control (FRC) selection signal to process display data for a moving image displayed on a display panel (Col. 26, Lines 23-50 teaches since sub-frames are used to process video the frame counter selects this gray-scale adjustment means including an intensity data arrangement switching means and a frame counter, which select, from a number of sub-frame groups (SF1 to SFn) having mutually differing sustained discharge periods (intensity weights), a number of sub-frames having predetermined numbers to make up one frame).

Thus it would have been obvious to one in the ordinary skill in the art at the time of invention was made to incorporate the teaching of Tahjima et al. in the teaching of Morita to be able to drive liquid crystal display device capable of efficiently supplying information and providing a correct gradation display without flickering (Col. 43, Lines 18-33).

Regarding Claim 10, Morita teaches (d) receiving data and, in response to the level of the liquid crystal polarity inversion signal, generating a segment voltage that drives a column electrode of the STN LCD (page 3, paragraph 63, page 12, paragraphs 241-248, page 13 paragraphs 248-250, page 15, paragraphs 300-308, page 16, paragraphs 311-317); and (f) receiving a row selection signal and, in response to the level of the liquid crystal polarity inversion signal, generating a row voltage that drives a row electrode of the STN LCD (page 3, paragraph 63, page 15, paragraphs 300-308, page 16, paragraphs 311-317).

Regarding Claim 11, Morita teaches n sub frames constitute one frame (page 3, paragraph 63, page 15, paragraphs 300-308, page 16, paragraphs 311-317).

Regarding Claim 13, Morita teaches one frame is comprised of n sub frames (page 3, paragraph 63, page 15, paragraphs 300-308, page 16, paragraphs 311-317).

Response to Arguments

7. Applicant's arguments, see remark, filed 12-08-2006, with respect to the rejection(s) of claim(s) 1 under 35 U.S.C. 103(a) Morita (US 2002/0196243 A1) in view of (Hirai et al. (5,953,002) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Morita (US 2002/0196243 A1) in view of Tajima et al. (US 6,249,265 B1).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Tajima et al. (5,818,419 Display device and method for driving the same.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prabodh M. Dharia whose telephone number is 571-272-7668. The examiner can normally be reached on M-F 8AM to 5PM.

10. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

11. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Any response to this action should be mailed to:

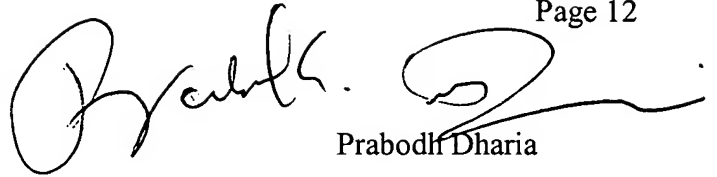
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Application/Control Number: 10/712,164

Art Unit: 2629

Page 12



Prabodh Dharia

Partial Signatory Authority Program

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